WHAT IS CLAIMED IS:

1. A computation device for finding tangent angles, comprising:

a signal input terminal for inputting a complex signal that includes a real part coefficient and an imaginary part coefficient;

a direct current input terminal for inputting a direct current signal;

a first real part subtractor having a positive input terminal, a negative input terminal and an output terminal, wherein a direct current signal is fed to the positive input terminal of the first real part subtractor, the real part coefficient is fed to the negative input terminal of the first real part subtractor, and subtraction result is output from the output terminal of the first real part subtractor;

a second real part subtractor having a positive input terminal, a negative input terminal and an output terminal, wherein the direct current signal is fed to the negative input terminal of the second real part subtractor, the real part coefficient is fed to the positive input terminal of the second real part subtractor, and the subtraction result is output from the output terminal of the second real part subtractor;

a first imaginary part subtractor having a positive input terminal, a negative input terminal and an output terminal, wherein the direct current signal is fed to the positive terminal of the first imaginary part subtractor, the imaginary part coefficient is fed to the negative terminal of the first imaginary part subtractor, and the subtraction result is output from the output terminal of the first imaginary part subtractor;

a second imaginary part subtractor having a positive input terminal, a negative input terminal and an output terminal, wherein the direct current signal is fed to the negative terminal of the second imaginary part subtractor, the imaginary part coefficient is fed to the positive terminal of the second imaginary part subtractor, and a subtraction

result is output from the output terminal of the second imaginary part subtractor;

a first comparator for comparing the direct current signal and the real part coefficient to produce a real part label;

a second comparator for comparing the direct current signal and the imaginary part coefficient to produce an imaginary part label;

a first multiplexer for selecting data either from the output terminal of the first real part subtractor or from the output terminal of the second real part subtractor according to the real part label and outputting an absolute real part value;

a second multiplexer for selecting data either from the output terminal of the first imaginary part subtractor or from the output terminal of the second imaginary part subtractor according to the imaginary part label and outputting an absolute imaginary part value;

an XOR logic gate for receiving the real part label and the imaginary part label and outputting an XORed logic output;

a third multiplexer having a first input terminal for receiving the absolute real part value, a second input terminal for receiving the absolute imaginary part value and an output terminal for outputting the absolute real part value or the absolute imaginary part value to serve as a horizontal axis value according to a result of XOR computation;

a fourth multiplexer having a first input terminal for receiving the absolute imaginary part value, a second input terminal for receiving the absolute real part value and an output terminal for outputting the absolute imaginary part value or the absolute real part value to serve as a vertical axis value according to the result of XOR computation;

an eight-bit divider for finding a tangent value by dividing the vertical axis

value by the horizontal axis value;

a shift encoder for generating a set of shift-encoded codes according to the real part label and the imaginary part label; and

an angle-computing device for finding a quantization value according to the tangent value and the shift-encoded codes.

2. The computation device of claim 1, wherein a quantized value obtained from the angle-computing device includes a five-bit length phase value and a two-bit length phase shift value.

3. A differential-encoding quadrant phase shift keying (DQPSK) system, comprising:

a tangent angle computation device having:

a direct current input terminal for inputting a direct current signal;

a first real part subtractor having a positive input terminal, a negative input terminal and an output terminal, wherein the direct current signal is fed to the positive input terminal of the first real part subtractor, a real part coefficient is fed to the negative input terminal of the first real part subtractor, and a subtraction result is output from the output terminal of the first real part subtractor;

a second real part subtractor having a positive input terminal, a negative input terminal and an output terminal, wherein the direct current signal is fed to the negative input terminal of the second real part subtractor, the real part coefficient is fed to the positive input terminal of the second real part subtractor, and a subtraction result is output from the output terminal of the second real part subtractor;

a first imaginary part subtractor having a positive input terminal, a negative input terminal and an output terminal, wherein the direct current signal is fed to the

positive terminal of the first imaginary part subtractor, an imaginary part coefficient is fed to the negative terminal of the first imaginary part subtractor, and a subtraction result is output from the output terminal of the first imaginary part subtractor;

a second imaginary part subtractor having a positive input terminal, a negative input terminal and an output terminal, wherein the direct current signal is fed to the negative input terminal of the second imaginary part subtractor, the imaginary part coefficient is fed to the positive input terminal of the second imaginary part subtractor, and a subtraction result is output from the output terminal of the second imaginary part subtractor;

a first comparator for comparing the direct current signal and the real part coefficient to produce a real part label;

a second comparator for comparing the direct current signal and the imaginary part coefficient to produce an imaginary part label;

a first multiplexer for selecting data either from the output terminal of the first real part subtractor or from the output terminal of the second real part subtractor according to the real part label and outputting an absolute real part value;

a second multiplexer for selecting data either from the output terminal of the first imaginary part subtractor or from the output terminal of the second imaginary part subtractor according to the imaginary part label and outputting an absolute imaginary part value;

an XOR logic gate for receiving the real part label and the imaginary part label and outputting an XORed logic output;

a third multiplexer having a first input terminal for receiving the absolute real part value, a second input terminal for receiving the absolute imaginary part value and

an output terminal for outputting the absolute real part value or the absolute imaginary part value to serve as a horizontal axis value according to a result of XOR computation;

a fourth multiplexer having a first input terminal for receiving the absolute imaginary part value, a second input terminal for receiving the absolute real part value and an output terminal for outputting the absolute imaginary part value or the absolute real part value to serve as a vertical axis value according to the result of XOR computation;

an eight-bit divider for finding a tangent value by dividing the vertical axis value by the horizontal axis value;

a shift encoder for generating a set of shift-encoded codes according to the real part label and the imaginary part label;

an angle-computing device for finding a quantization value according to the tangent value and the shift-encoded codes;

and

a DQPSK decoder for receiving the quantized angle and decoding the complex signal according to a quantized value.

4. The DQPSK decoding system of claim 3, wherein the quantized value obtained from the angle-computing device includes a five-bit length phase value and a two-bit length phase shift value.